

FIG . 1

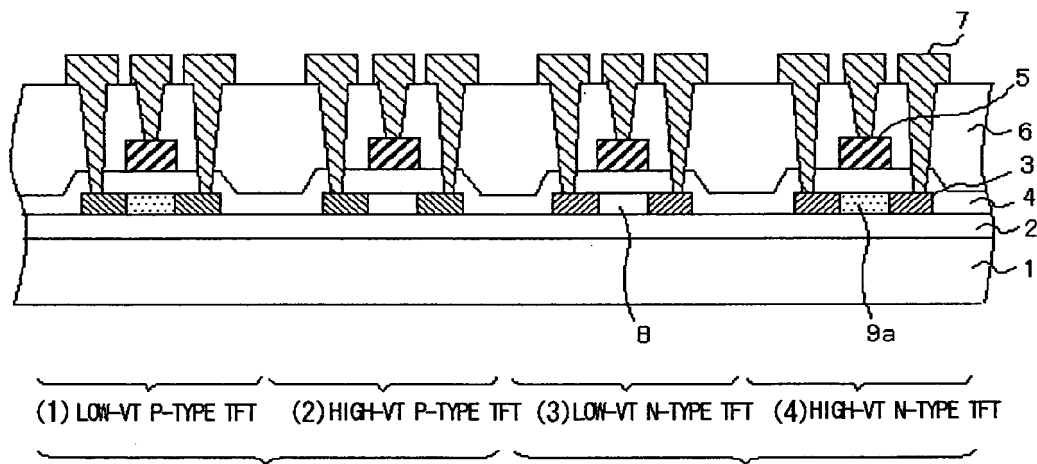


FIG . 2a

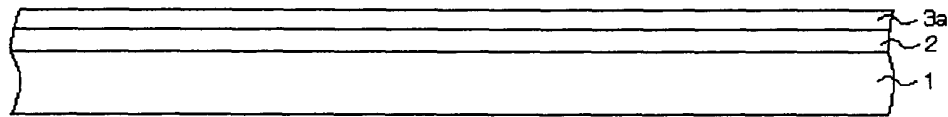


FIG . 2b

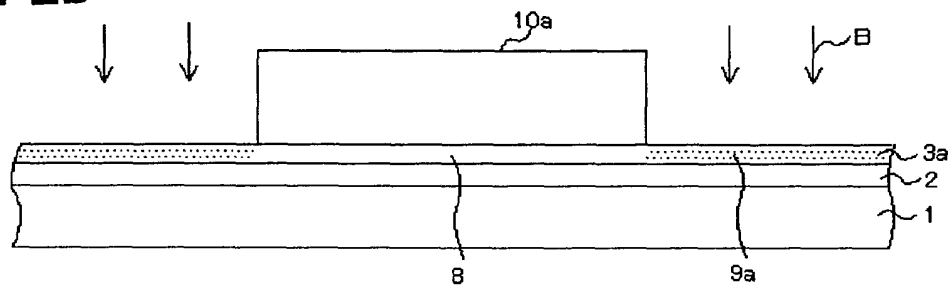


FIG . 2c

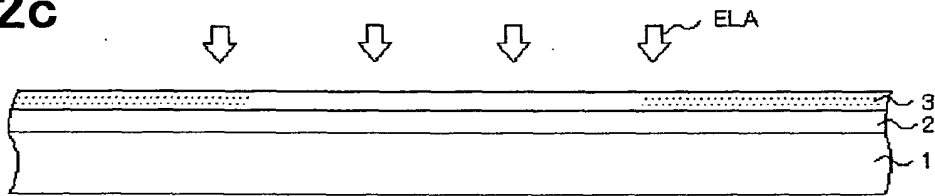


FIG . 2d

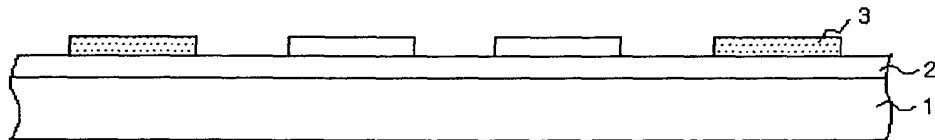


FIG . 2e

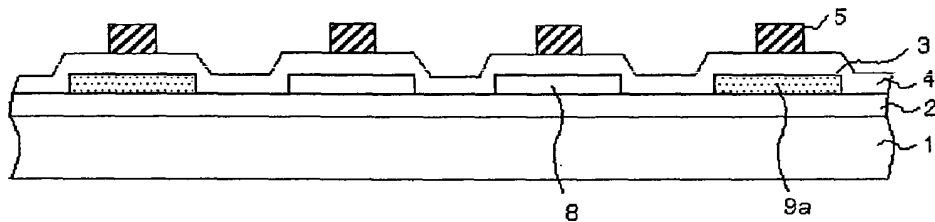


FIG . 3a

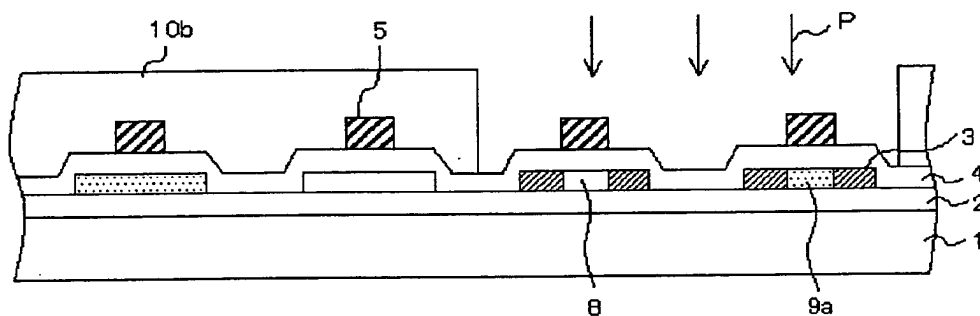


FIG . 3b

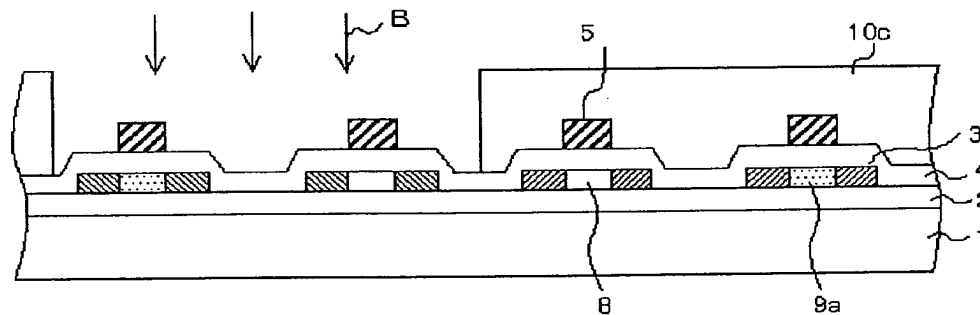


FIG . 3c

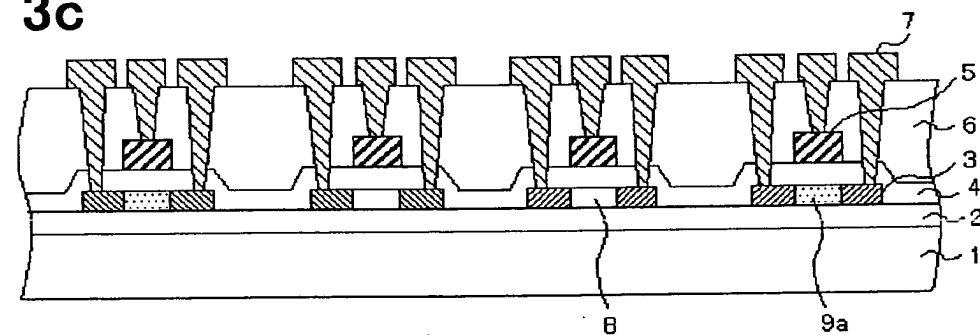


FIG . 4

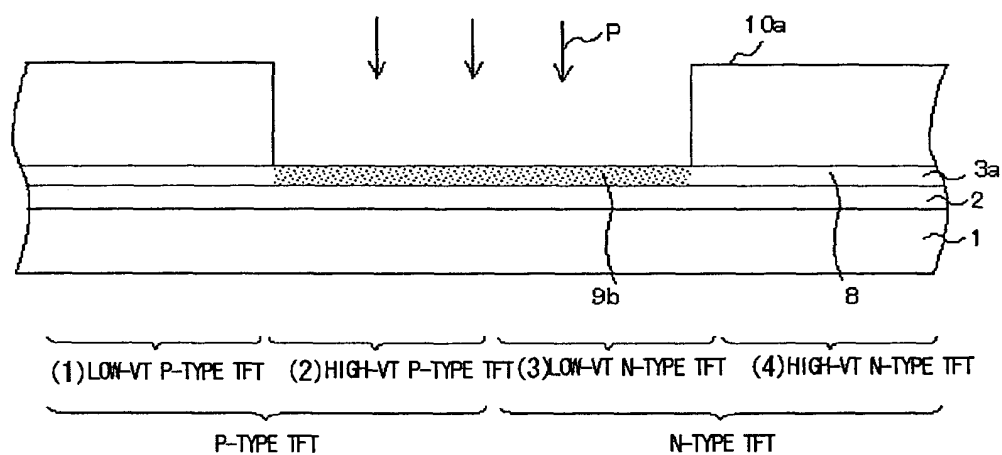


FIG . 5a

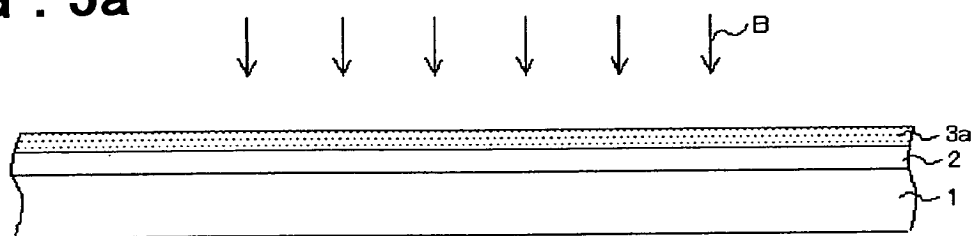


FIG . 5b

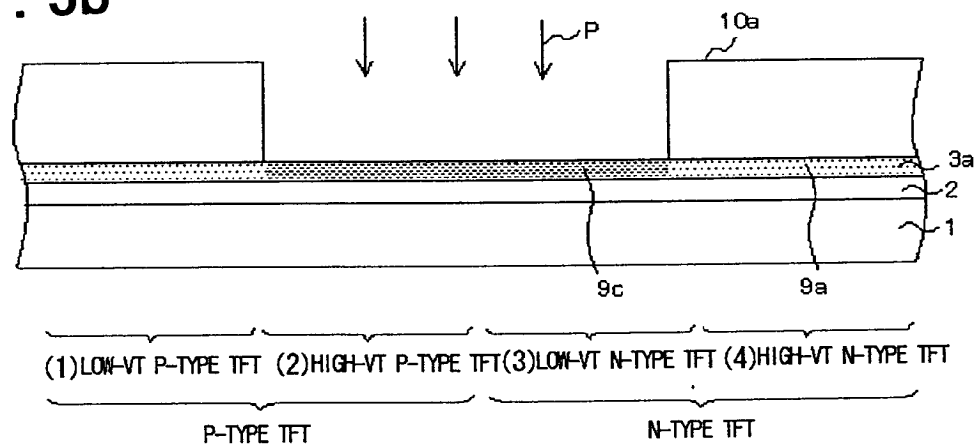


FIG . 6a

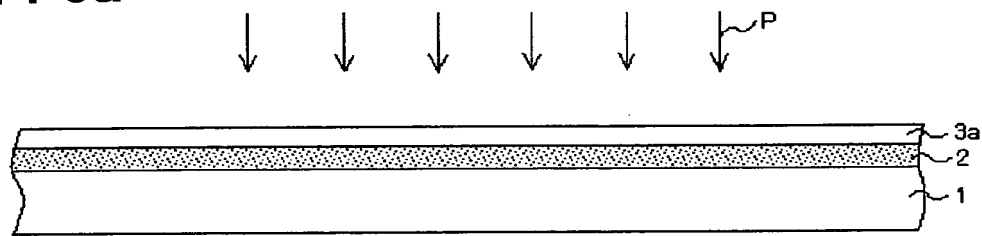


FIG . 6b

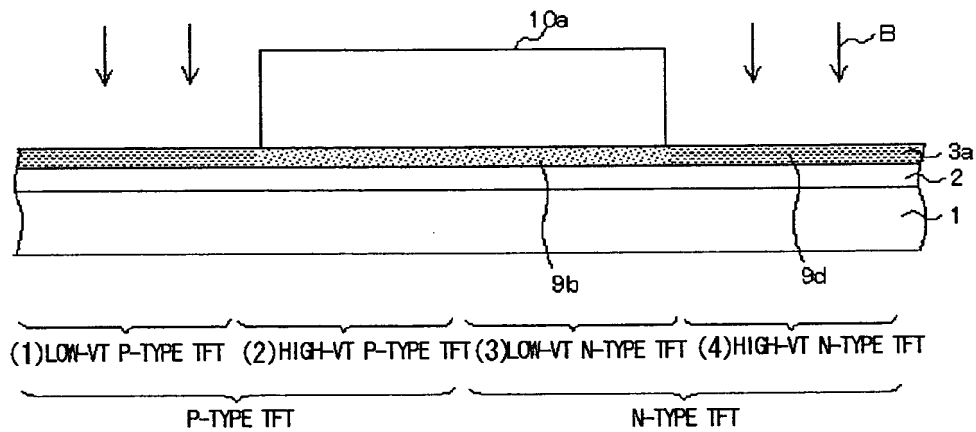


FIG . 7

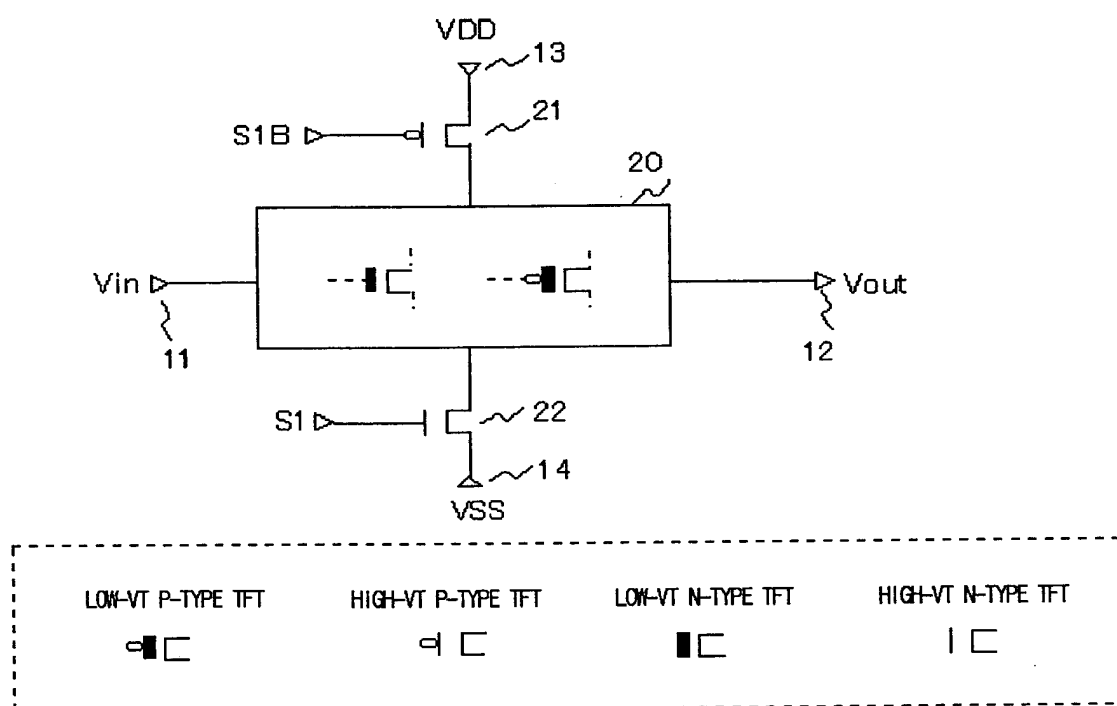


FIG . 8

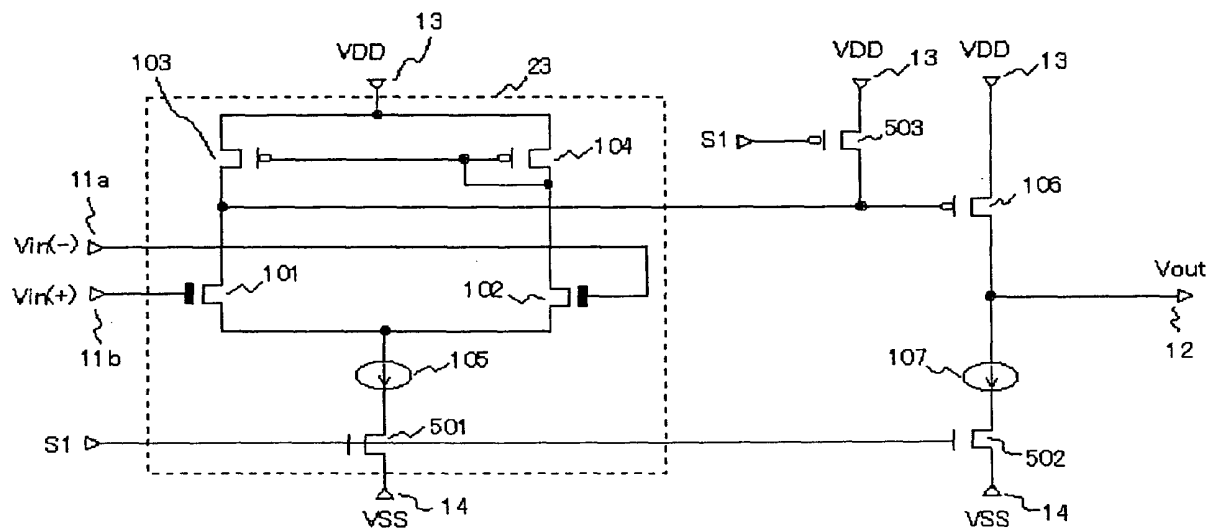




FIG . 9

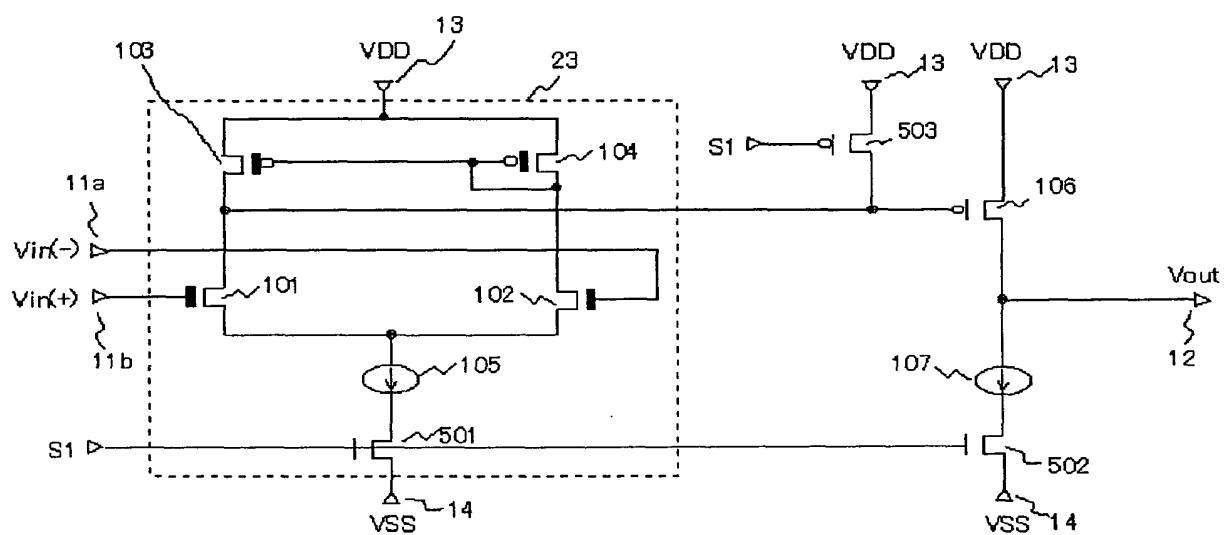


FIG. 10

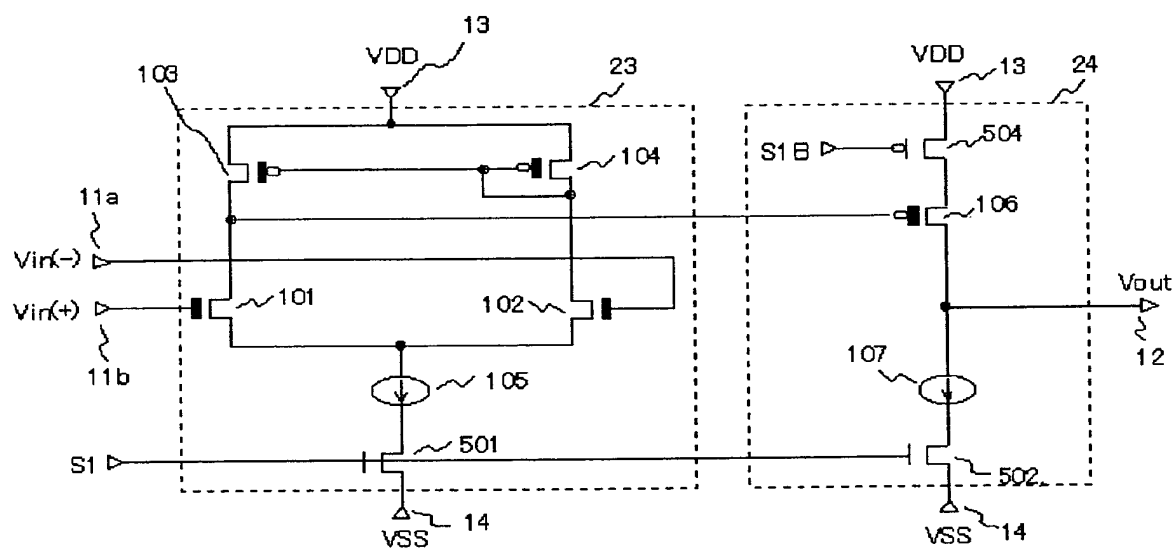


FIG. 11

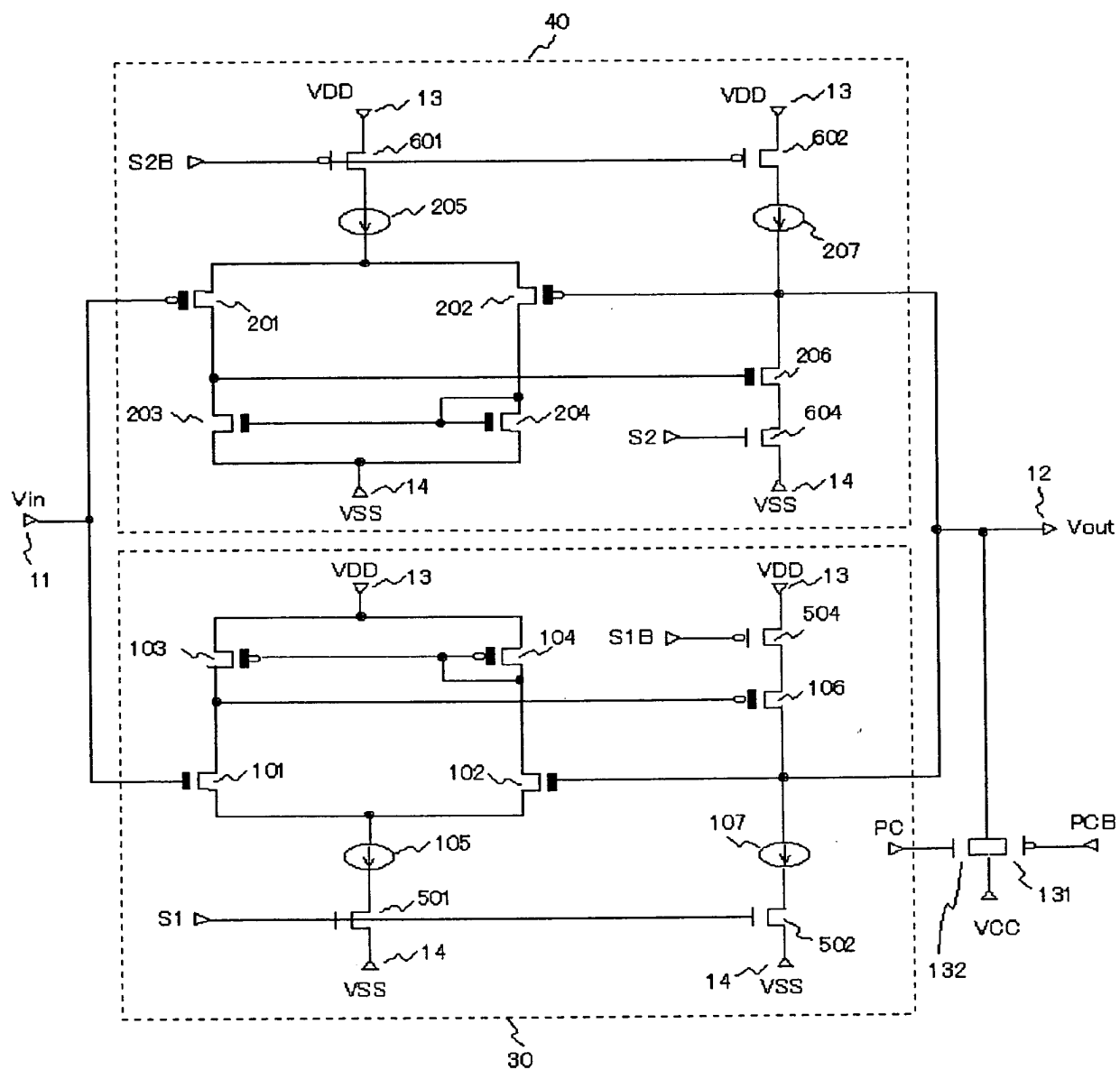


FIG . 12

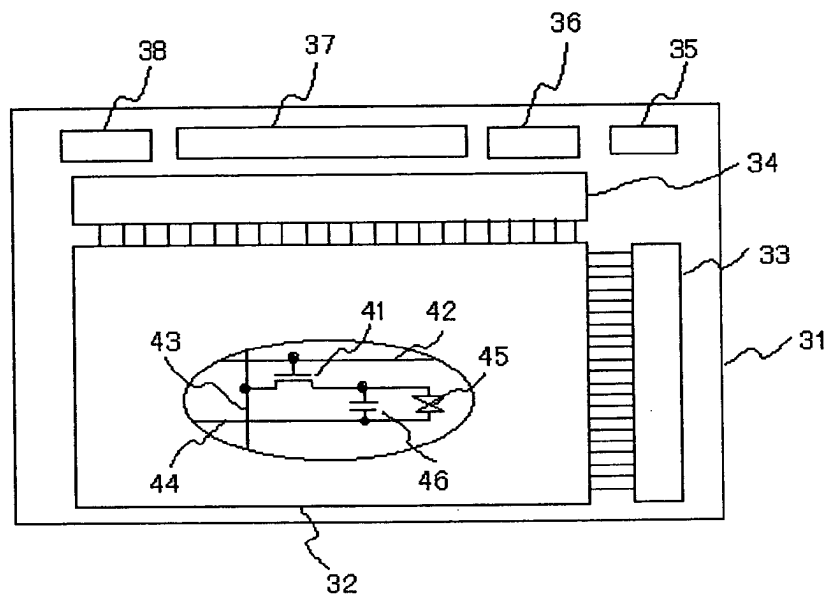


FIG . 13

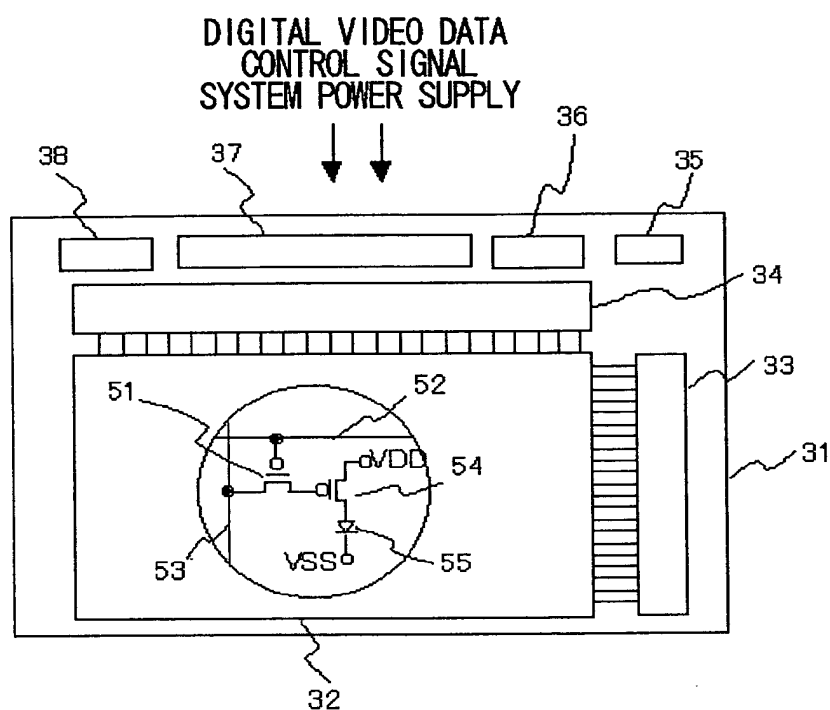


FIG .14

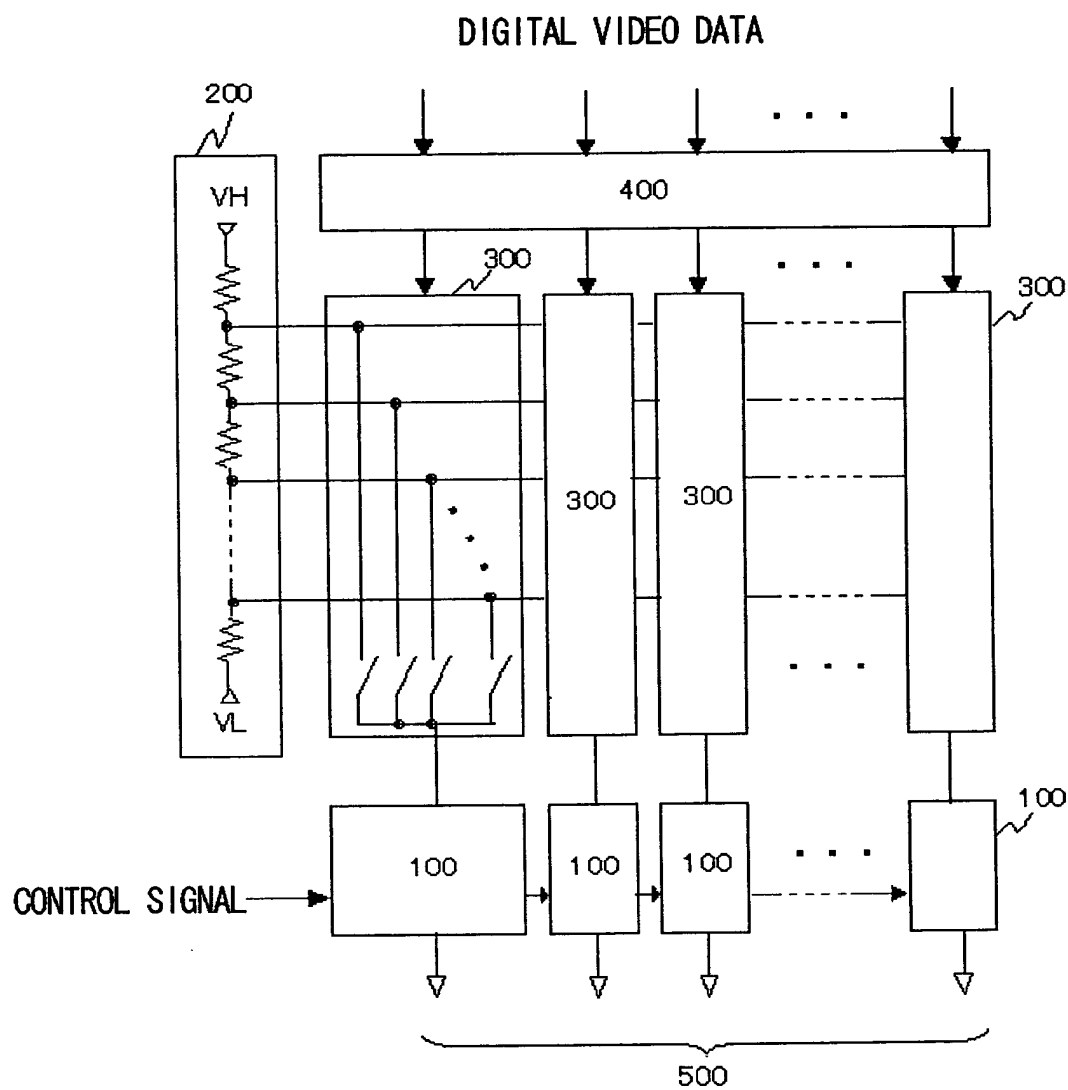


FIG .15

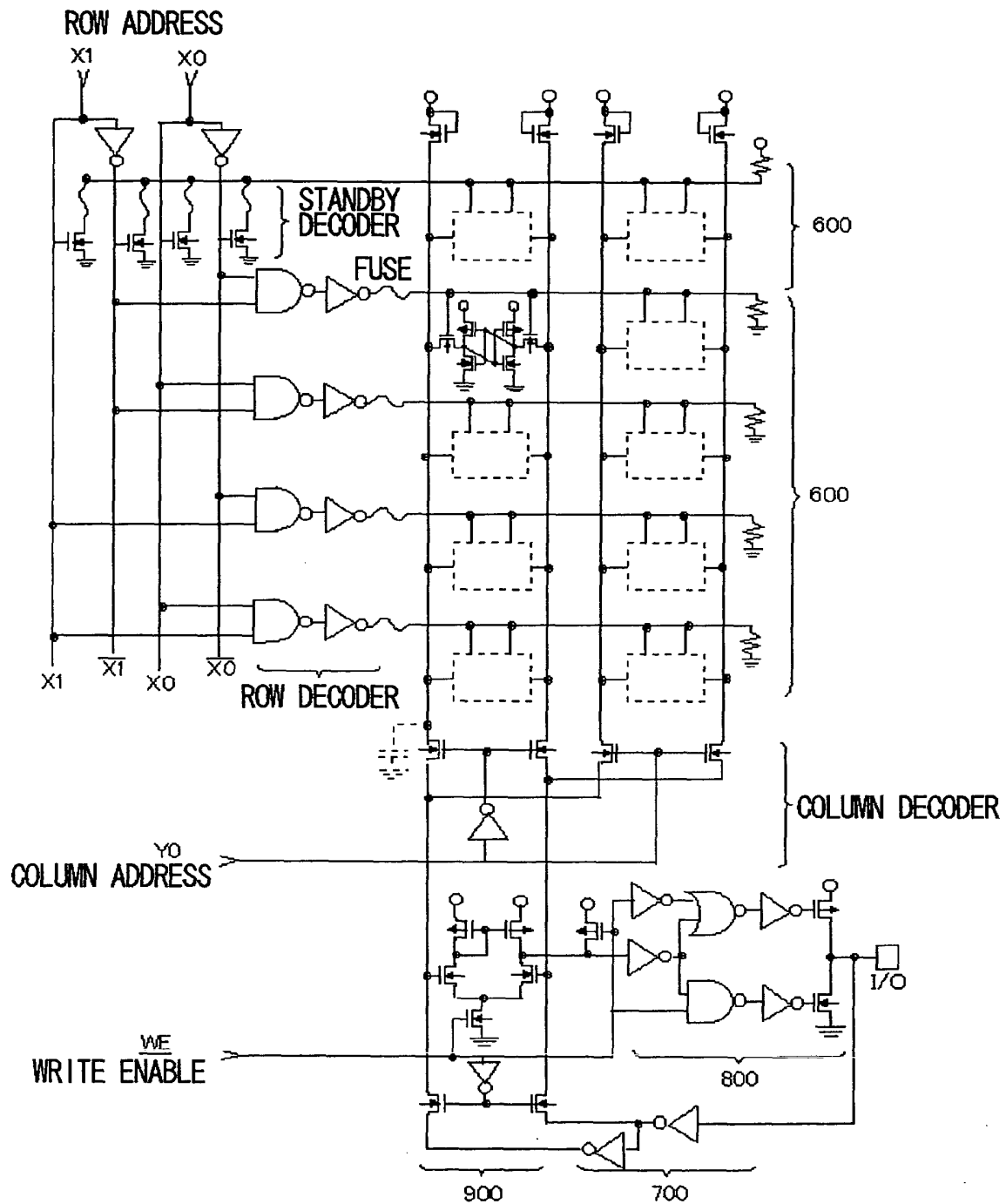


FIG . 16a

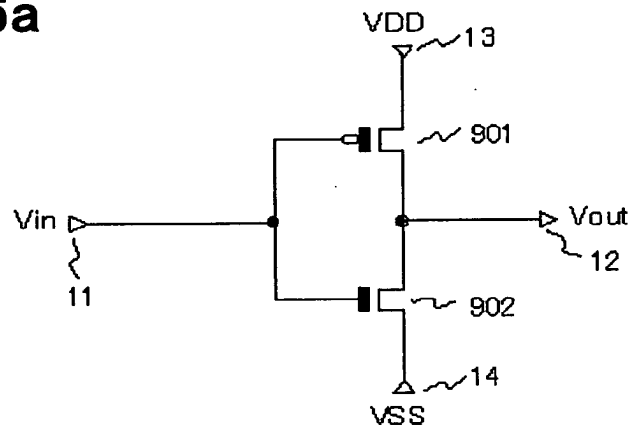


FIG . 16b

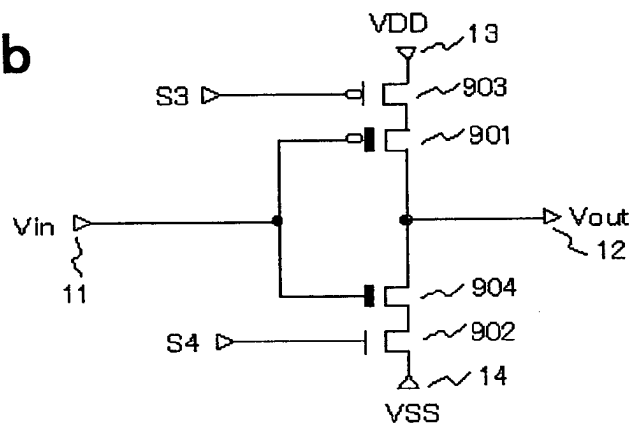
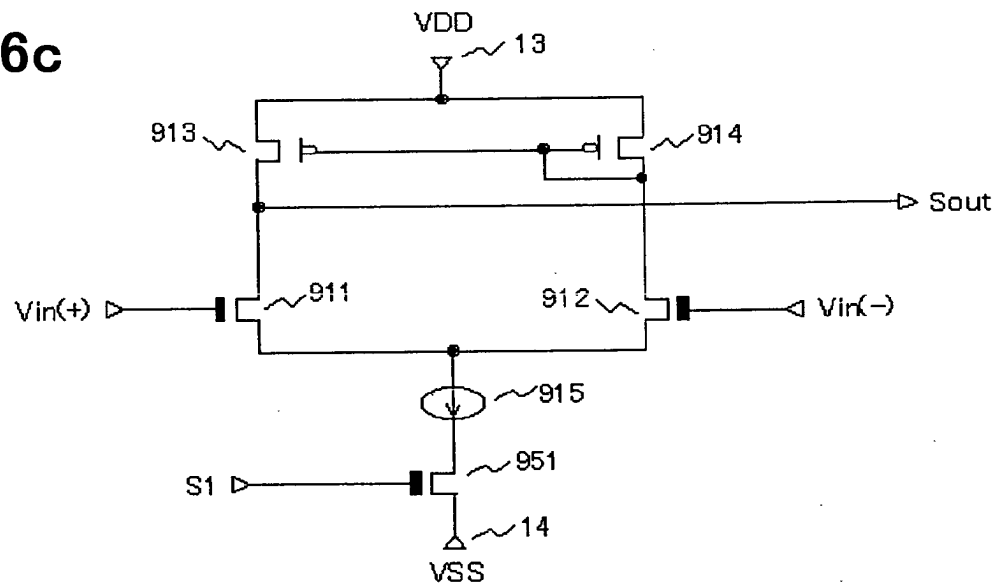


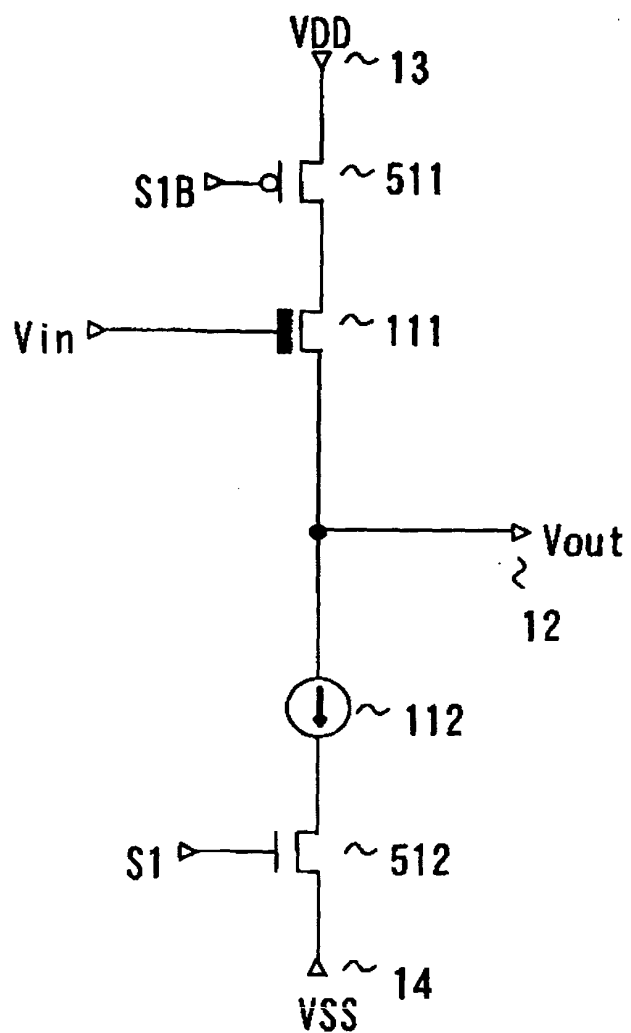
FIG . 16c





[illegible]

FIG . 18



The circuit diagram shows a differential amplifier. The top half consists of two PMOS transistors, labeled  $\sim 103$  and  $104$ , whose gates are connected to  $V_{DD} \sim 13$ . The source of transistor  $104$  is connected to its gate, forming a diode-connected load. The sources of both PMOS transistors are connected to a common node, which is the output of the amplifier. The bottom half consists of two NMOS transistors, labeled  $\sim 101$  and  $102$ . The gates of both NMOS transistors are connected to a common input signal  $V_{in}(+)$ , indicated by a wavy line and label  $11b$ . The gates of both NMOS transistors are also connected to a bias voltage  $V_{B1}$ . The sources of both NMOS transistors are connected to a common tail node, which is connected to  $V_{SS} \sim 14$  through a tail current source transistor  $\sim 105$ . The gates of the tail current source transistor  $105$  and the NMOS transistors  $101$  and  $102$  are connected to a common input signal  $V_{in}(-)$ , indicated by a wavy line and label  $11a$ . The gates of the tail current source transistor  $105$  and the NMOS transistors  $101$  and  $102$  are also connected to a bias voltage  $V_{B1}$ . The sources of both NMOS transistors are connected to a common tail node, which is connected to  $V_{SS} \sim 14$  through a tail current source transistor  $\sim 105$ .

FIG . 20

